Low-Voltage, Single and Dual Supply, Triple SPDT Analog Switch

The Intersil ISL43231 device is a precision, bidirectional, analog switch configured as a a triple single pole/double throw (SPDT) switch, designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. The device has an inhibit and inhibit bar pin to simultaneously open all signal paths. The device also has a latch bar pin to lock in the last switch address.

ON-resistance of 39Ω with a ±5V supply and 125Ω with a +3.3V supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 2.5nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single +3.3V or +5V supply or dual ±5V supplies.

The ISL43231 is a committed triple SPDT, which is perfect for use in 2-to-1 multiplexer applications. Table 1 summarizes the performance of this part.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	TRIPLE SPDT
±5V R_{ON}	39Ω
±5V t_{ON}/t_{OFF}	32ns/18ns
12V R_{ON}	32Ω
12V t_{ON}/t_{OFF}	23ns/15ns
5V R_{ON}	65Ω
5V t_{ON}/t_{OFF}	38ns/19ns
3.3V R_{ON}	125Ω
3.3V t_{ON}/t_{OFF}	70ns/32ns
Package	20 Ld 4x4 QFN

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”
- Application Note AN520 “CMOS Analog Multiplexers and Switches; Specifications and Application Considerations.”
- Application Note AN1034 “Analog Switch and Multiplexer Applications”

Features

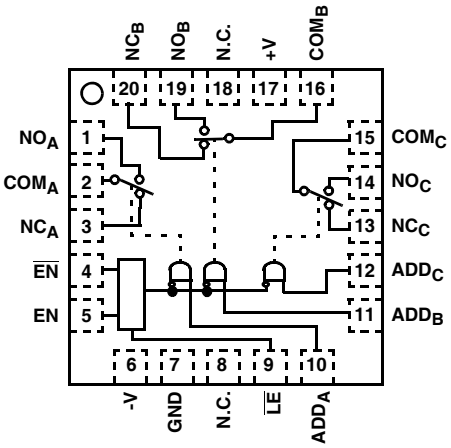
- Specified at 3.3V, 5V, ±5V, and 12V Supplies for 10% Tolerances
- ON-resistance (R_{ON}) Max, V_S = ±4.5V 50Ω
- ON-resistance (R_{ON}), V_S = +3V 135Ω
- R_{ON} Matching Between Channels, V_S = ±5V. . . . . <2Ω
- Low Charge Injection, V_S = ±5V 0.3pC
- Single Supply Operation. . . . . +2V to +12V
- Dual Supply Operation . . . . . ±2V to ±6V
- Fast Switching Action (V_S = +5V)
  - t_{ON} 38ns
  - t_{OFF} 19ns
- Guaranteed Max Off-leakage 2.5nA
- Break-Before-Make
- TTL, CMOS Compatible
- Pb-Free (RoHS Compliant)

Applications

- Battery Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners (MRI)
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinout

ISL43231
(20 LD QFN)
TOP VIEW



Truth Table

ISL43231						
$\overline{LE}$	EN	$\overline{EN}$	ADD_C	ADD_B	ADD_A	SWITCH ON
0	1	0	X	X	X	Last Switches Selected
X	0	X	X	X	X	NONE
X	X	1	X	X	X	NONE
1	1	0	X	X	0	NC_A
1	1	0	X	X	1	NO_A
1	1	0	X	0	X	NC_B
1	1	0	X	1	X	NO_B
1	1	0	0	X	X	NC_C
1	1	0	1	X	X	NO_C

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V, with V+ between 2.7V and 10V.
X = Don't Care.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL43231IRZ*	43 231IRZ	-40 to +85	20 Ld QFN	L20.4x4

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
$\overline{EN}$	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
EN	Digital Control Input. Connect to V+ for Normal Operation. Connect to GND to turn all switches off.
$\overline{LE}$	Digital Control Input. Connect to +V for Normal Operation. Connect to GND to latch the last switch state.
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
ADD	Address Input Pin
N.C.	No Internal Connection

Absolute Maximum Ratings

V+ to V- . . . . . -0.3V to15V
V+ to GND . . . . . -0.3V to15V
V- to GND. . . . . -15V to 0.3V
Input Voltages
  $\overline{LE}$, $\overline{EN}$, EN, NO, NC, ADD (Note 1). . . ((V-) -0.3) to ((V+) + 0.3V)
Output Voltages
  COM (Note 1). . . . . ((V-) -0.3) to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . . ±30mA
Peak Current NO, NC, or COM
  (Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating
  HBM (Per Mil-STD-883, Method 3015.7) . . . . . >2.5kV

Thermal Information

Thermal Resistance (Typical, Notes 2, 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld 4x4 QFN Package	45	8

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Pb-Free Reflow Profile. . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Signals on NC, NO, COM, ADD, EN, $\overline{EN}$, or $\overline{LE}$ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**V-**	-	**V+**	V
ON Resistance, R_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V (See Figure 7)	25	-	44	50	Ω
		Full	-	-	**80**	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V (Note 6)	25	-	1.3	4	Ω
		Full	-	-	**6**	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = ±3V, 0V (Note 7)	25	-	7.5	9	Ω
		Full	-	-	**12**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V (Note 7)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V (Note 7)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V (Note 7)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	**2.4**	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	**0.8**	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{ENH}}$, $I_{\overline{ENL}}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	**-0.5**	-	**0.5**	µA
Input Current, I_{ENH}, $I_{\overline{LEH}}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	**-1.5**	-	**1.5**	µA
Input Current, I_{ENL}, $I_{\overline{LEL}}$	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	**-4**	-	**4**	µA

Electrical Specifications - 5V Supply Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)	25	-	35	-	ns
		Full	-	45	-	ns
Enable Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)	25	-	22	-	ns
		Full	-	27	-	ns
Address Transition Time, t_{TRANS}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)	25	-	43	-	ns
		Full	-	53	-	ns
Break-Before-Make Time, t_{BBM}	V_S = ±5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	-	7	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	-	25	-	ns
		Full	-	35	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	-	0	-	ns
		Full	-	0	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	-	15	-	ns
		Full	-	25	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.3	-	pC
NO/NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	25	-	3	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	25	-	9	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	25	-	14	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} or V_{NCx} = $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk (Note 8)		25	-	<-110	-	dB
All Hostile Crosstalk (Note 8)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	±**2**	-	±**6**	V
Positive Supply Current, I+	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	**-7**	-	**7**	µA
Negative Supply Current, I-		Full	**-1**	-	**1**	µA

NOTES:

4. V_{IN} = Input logic voltage to configure the device in a given state.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. $\Delta R_{ON} = R_{ON}$ (MAX) - R_{ON} (MIN).
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Between any two switches.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Electrical Specifications +12V Supply

Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, R_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (See Figure 6)	25	-	37	45	Ω
		Full	-	-	**55**	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (Note 6)	25	-	1.2	2	Ω
		Full	-	-	**2**	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V (Note 7)	25	-	5	7	Ω
		Full	-	-	**7**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13.2V, V_{COM} = 12V, 1V, V_{NO} or V_{NC} = 1V, 12V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V, or floating (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	**3.7**	3.3	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	2.7	**0.8**	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{ENH}}$, $I_{\overline{ENL}}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	**-0.5**	-	**0.5**	µA
Input Current, I_{ENH}, $I_{\overline{LEH}}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	**-1.5**	-	**1.5**	µA
Input Current, I_{ENL}, $I_{\overline{LEL}}$	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	**-4**	-	**4**	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	24	-	ns
		Full	-	29	-	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	15	-	ns
		Full	-	20	-	ns
Address Transition Time, t_{TRANS}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4 (See Figure 1)	25	-	27	-	ns
		Full	-	32	-	ns
Break-Before-Make Time Delay, t_D	V+ = 13.2V, R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 10V, V_{IN} = 0 to 4 (See Figure 3)	Full	-	5	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	-	25	-	ns
		Full	-	35	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	-	0	-	ns
		Full	-	0	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	-	15	-	ns
		Full	-	25	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	2.7	-	pC

Electrical Specifications +12V Supply

Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} or V_{NCx}= $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk (Note 8)		25	-	<-110	-	dB
All Hostile Crosstalk (Note 8)		25	-	-105	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	25	-	3	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	25	-	9	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 8)	25	-	14	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	**2**	-	**12**	V
Positive Supply Current, I+	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+, all channels on or off	Full	**-7**	-	**7**	µA

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V (See Figure 6)	25	-	81	90	Ω
		Full	-	-	**120**	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V (Note 6)	25	-	2.2	4	Ω
		Full	-	-	**6**	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V (Note 7)	25	-	11.5	17	Ω
		Full	-	-	**24**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} or V_{NC} = 4.5V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	**2.4**	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	**0.8**	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{ENH}}$, $I_{\overline{ENL}}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	**-0.5**	-	**0.5**	µA
Input Current, I_{ENH}, $I_{\overline{LEH}}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	**-1.5**	-	**1.5**	µA
Input Current, I_{ENL}, $I_{\overline{LEL}}$	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	**-4**	-	**4**	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	43	-	ns
		Full	-	53	-	ns

Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
Enable Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	20	-	ns
		Full	-	25	-	ns
Address Transition Time, t_{TRANS}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	51	-	ns
		Full	-	56	-	ns
Break-Before-Make Time, t_{BBM}	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	-	9	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	-	25	-	ns
		Full	-	35	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	-	0	-	ns
		Full	-	0	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	-	15	-	ns
		Full	-	25	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.6	-	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} or V_{NCx}= $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk (Note 8)		25	-	<-110	-	dB
All Hostile Crosstalk (Note 8)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	**2**	-	**12**	V
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	**-7**	-	**7**	µA

Electrical Specifications 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

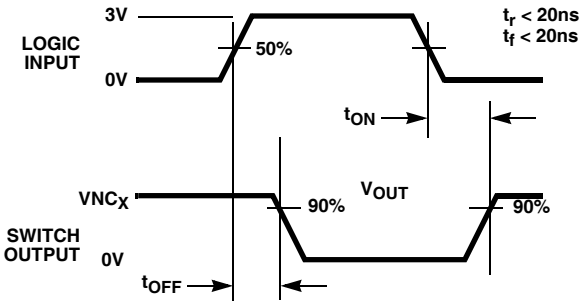
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON Resistance, R_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (See Figure 6)	25	-	135	-	Ω
		Full	-	155	-	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (Note 6)	25	-	3.4	-	Ω
		Full	-	5.4	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1V, 2V (Note 7)	25	-	34	-	Ω
		Full	-	44	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 3V, 1V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 3V, 1V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} or V_{NC} = 3V (Note 8)	25	-	0.002	-	nA
		Full	**-2.5**	-	**2.5**	nA

Electrical Specifications 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

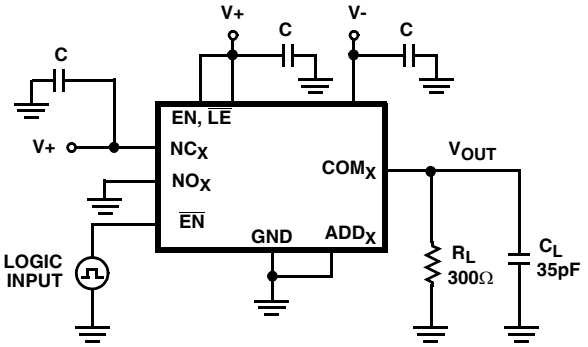
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 9)	TYP	MAX (Notes 5, 9)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	**2.4**	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	**0.8**	V
Input Current, I_{ADDH}, I_{ADDL}, $I_{\overline{ENH}}$, $I_{\overline{ENL}}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	**-0.5**	-	**0.5**	µA
Input Current, I_{ENH}, $I_{\overline{LEH}}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	**-1.5**	-	**1.5**	µA
Input Current, I_{ENL}, $I_{\overline{LEL}}$	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	**-4**	-	**4**	µA
DYNAMIC CHARACTERISTICS						
Enable Turn-ON Time, t_{ON}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	82	-	ns
		Full	-	102	-	ns
Enable Turn-OFF Time, t_{OFF}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	37	-	ns
		Full	-	47	-	ns
Address Transition Time, t_{TRANS}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 1)	25	-	96	-	ns
		Full	-	121	-	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (See Figure 3)	Full	-	13	-	ns
Latch Setup Time, t_S	(See Figure 4)	25	-	50	-	ns
		Full	-	60	-	ns
Latch Hold Time, t_H	(See Figure 4)	25	-	0	-	ns
		Full	-	0	-	ns
Latch Pulse Width, t_{WPW}	(See Figure 4)	25	-	30	-	ns
		Full	-	40	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	0.3	-	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} or V_{NCx}= $1V_{RMS}$ (See Figures 5, 7 and 20)	25	-	92	-	dB
Crosstalk, Note 8		25	-	<-110	-	dB
All Hostile Crosstalk, Note 8		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	**2**	-	**12**	V
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	Full	**-7**	-	**7**	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

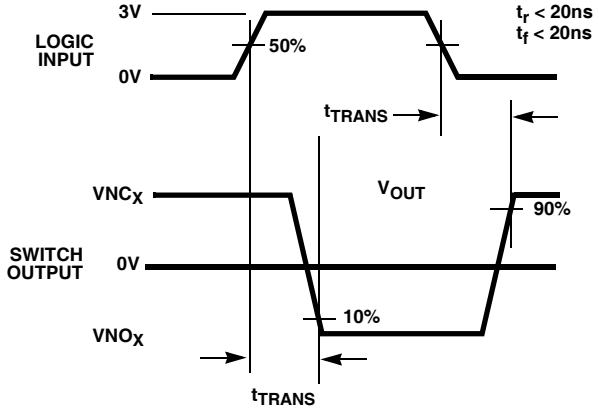
FIGURE 1A. ENABLE t_{ON} / t_{OFF} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

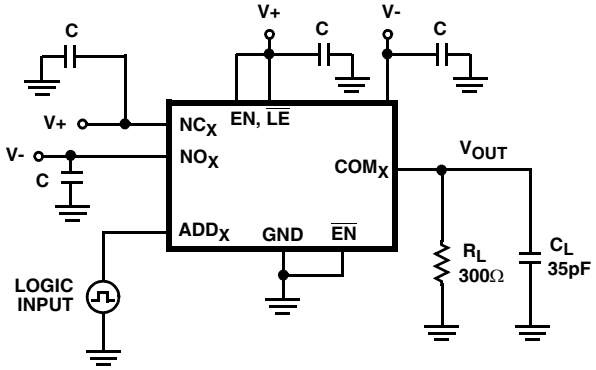
$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. ENABLE t_{ON} / t_{OFF} TEST CIRCUIT



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

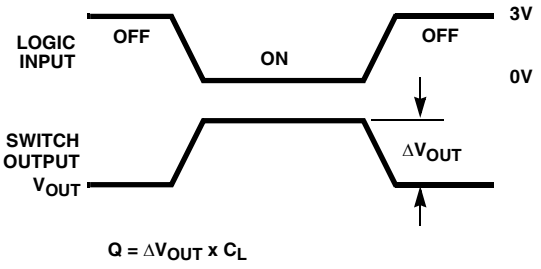
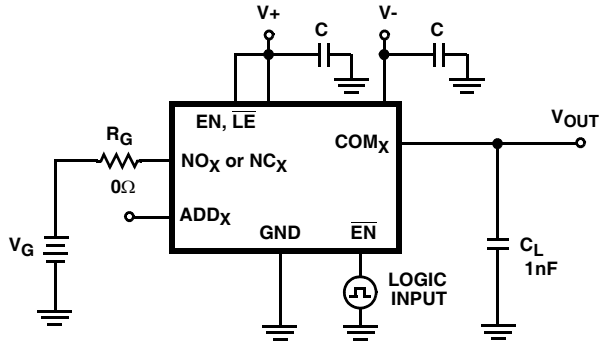


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

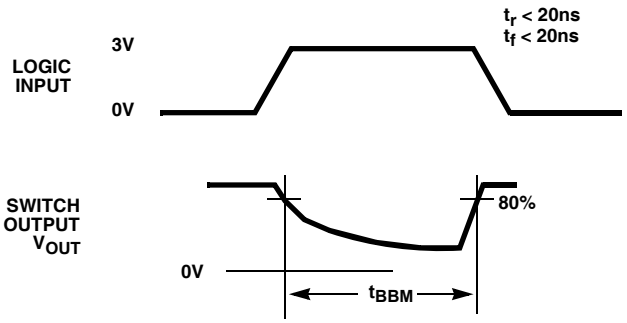
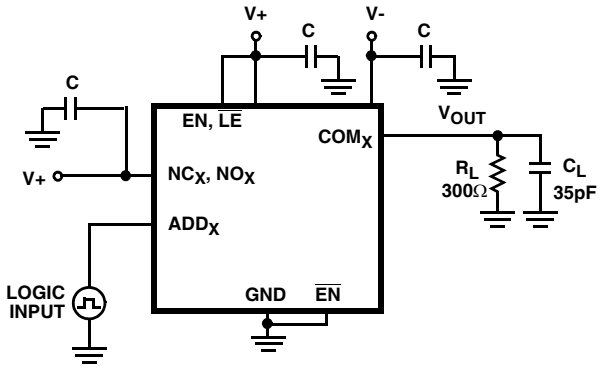


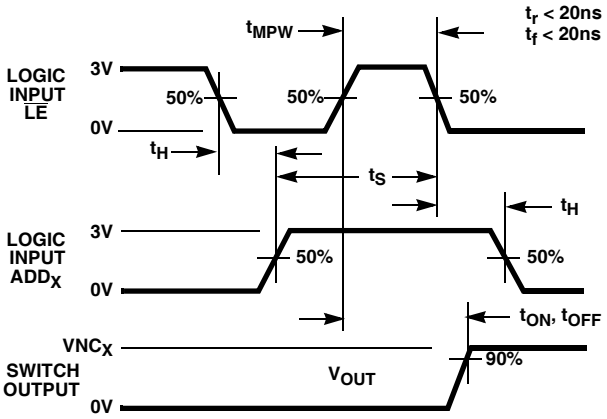
FIGURE 3A. t_{BBM} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

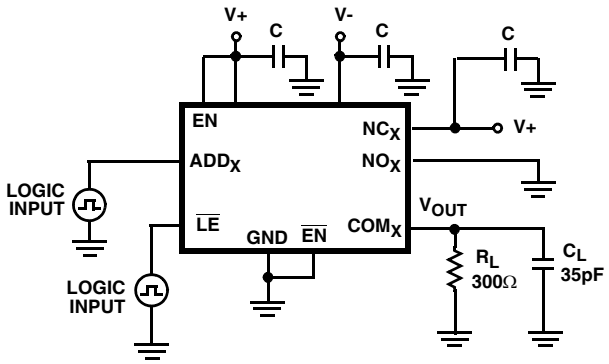
FIGURE 3B. t_{BBM} TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 4A. LATCH t_S, t_H, t_{MPW} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 4B. LATCH t_S, t_H, t_{MPW} TEST CIRCUIT

FIGURE 4. LATCH SETUP AND HOLD TIMES

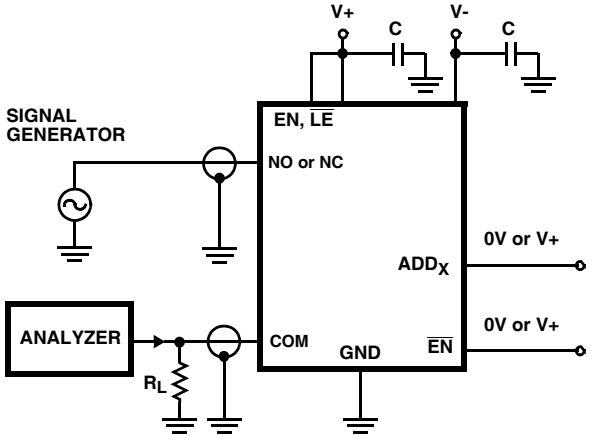


FIGURE 5. OFF ISOLATION TEST CIRCUIT

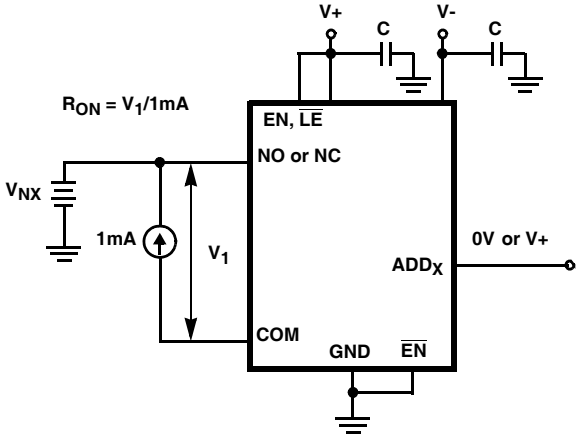


FIGURE 6. R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

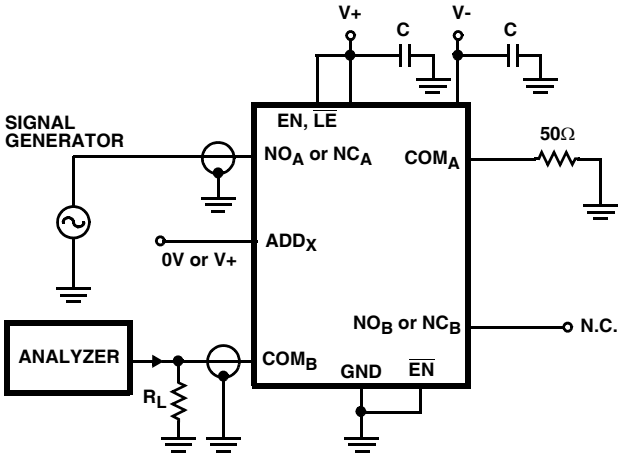


FIGURE 7. CROSSTALK TEST CIRCUIT

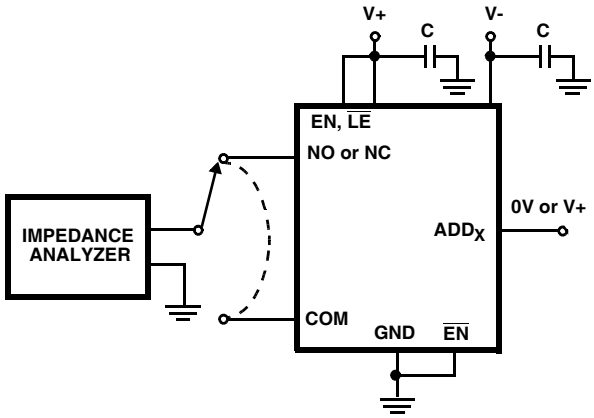


FIGURE 8. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43231 analog switch offers a precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low ON-resistance (39Ω) and high speed operation (t_{ON} = 38ns, t_{OFF} = 19ns) with dual 5V supplies.

It has an inhibit and inhibit bar pin to simultaneously open all signal paths. It also has a latch bar pin to lock in the last switch address.

The device is especially well suited for applications using ±5V supplies. With ±5V supplies, the performance (R_{ON}, Leakage, Charge Injection, etc.) is best in class.

High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 9). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 9). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 9). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

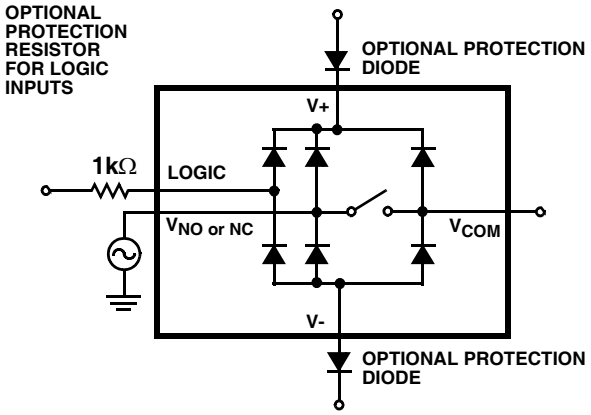


FIGURE 9. INPUT OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43231 construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL43231 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This switch device performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V or ±2V. It is important to

note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance Curves* for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.7V to 10V. At 12V the V_{IH} level is about 3.3V. This is still below the CMOS guaranteed high output minimum level of 4V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 4V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figures 18 and 19). Figures 18 and 19 also illustrates that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 20 details the high Off Isolation and Crosstalk rejection provided by this family. At 10MHz, Off Isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

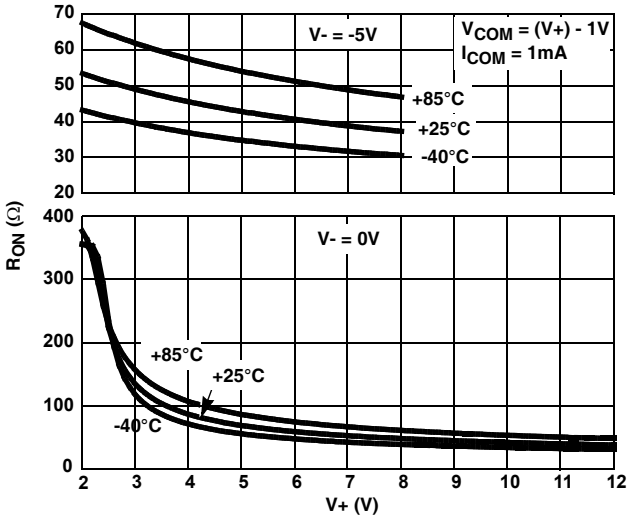


FIGURE 10. ON-RESISTANCE vs SUPPLY VOLTAGE

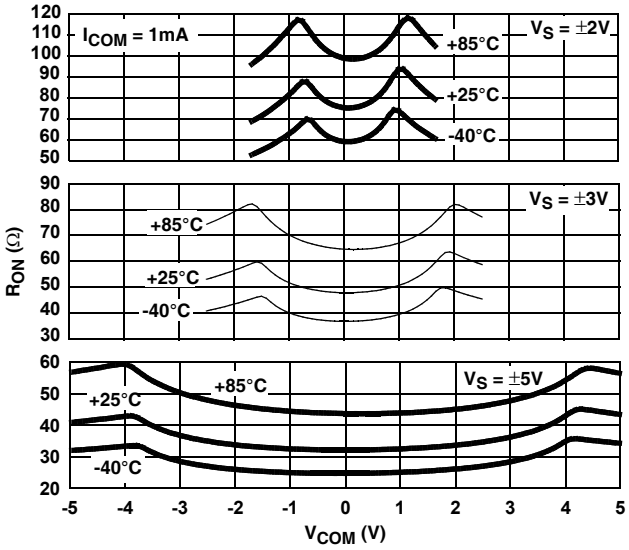


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

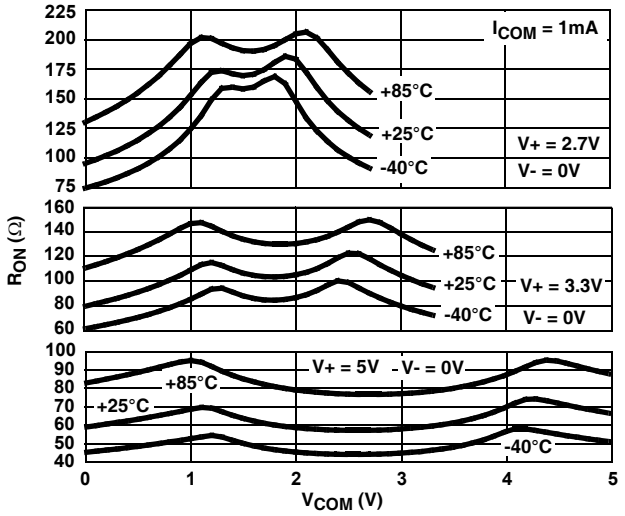


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

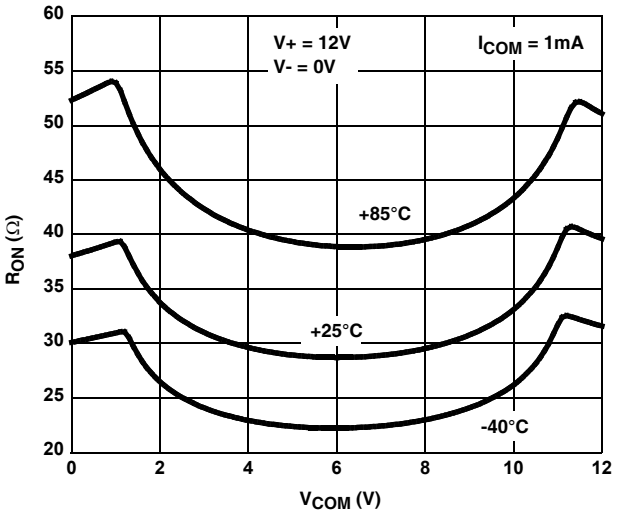


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

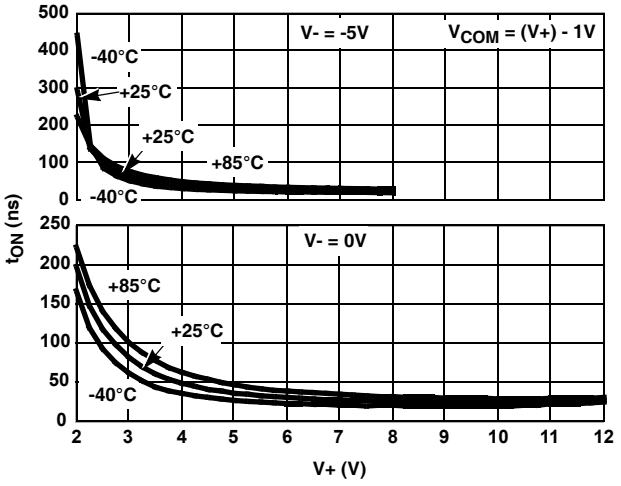


FIGURE 14. ENABLE TURN - ON TIME vs SUPPLY VOLTAGE

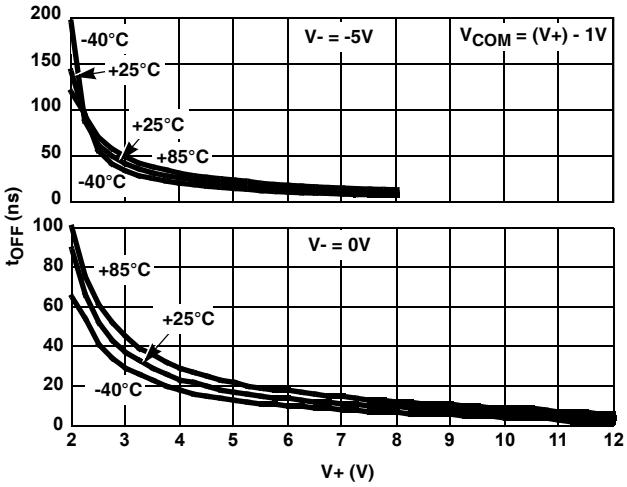


FIGURE 15. ENABLE TURN - OFF TIME vs SUPPLY VOLTAGE

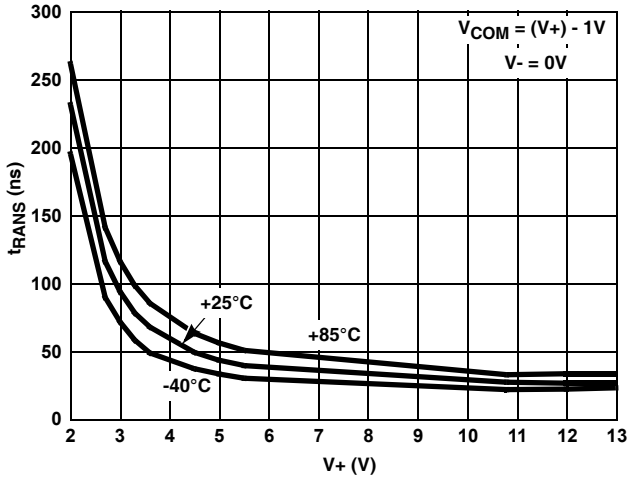


FIGURE 16. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

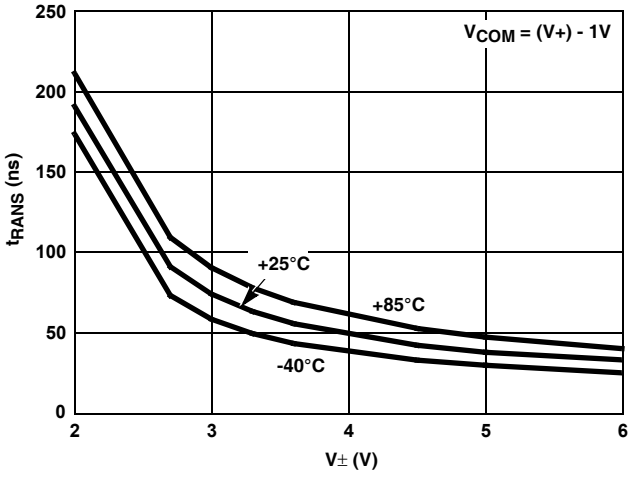


FIGURE 17. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

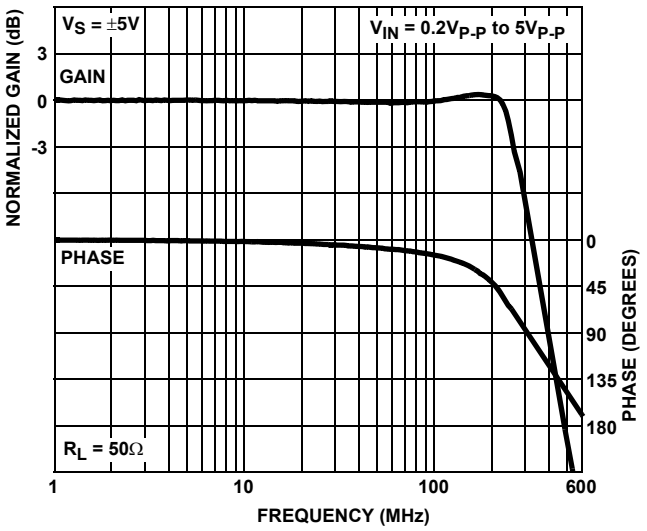


FIGURE 18. FREQUENCY RESPONSE

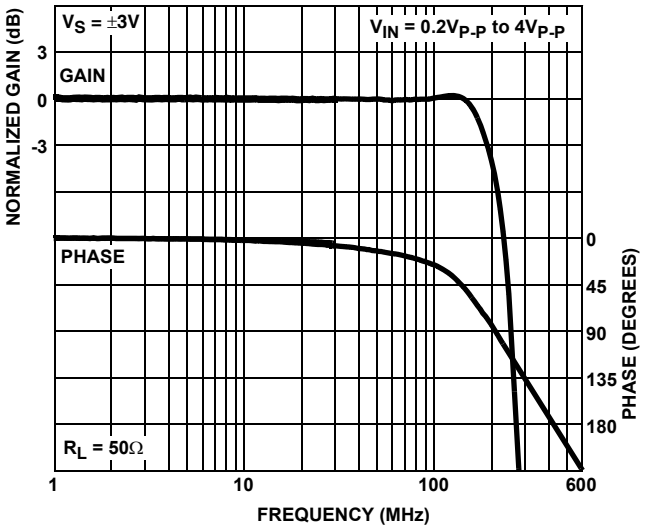


FIGURE 19. FREQUENCY RESPONSE

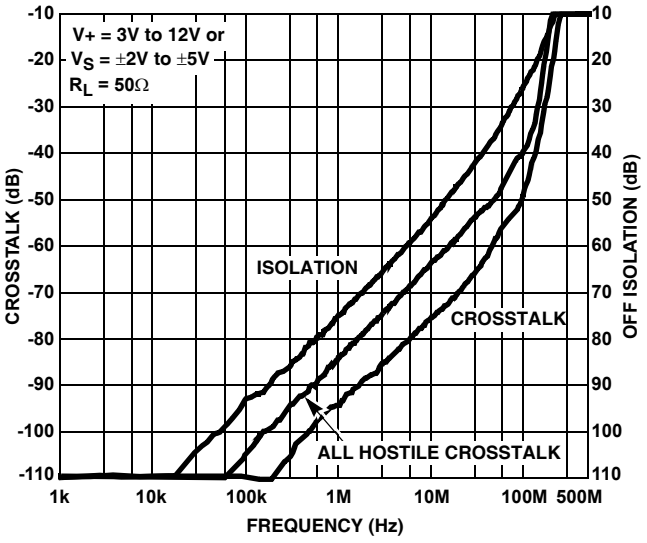


FIGURE 20. CROSSTALK AND OFF ISOLATION

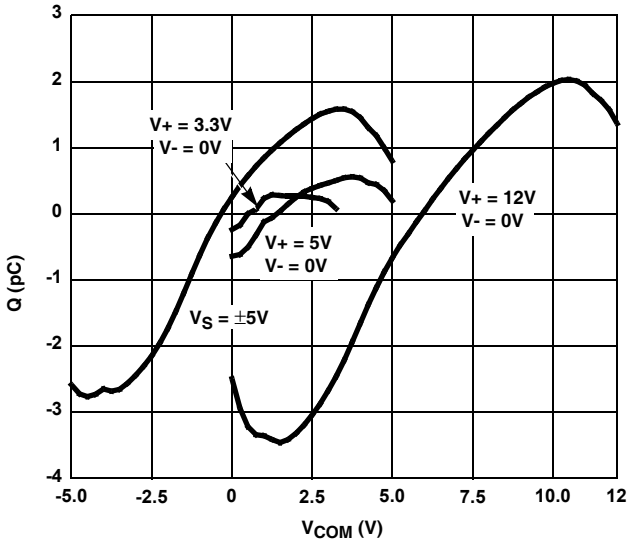


FIGURE 21. CHARGE INJECTION vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

193

PROCESS:

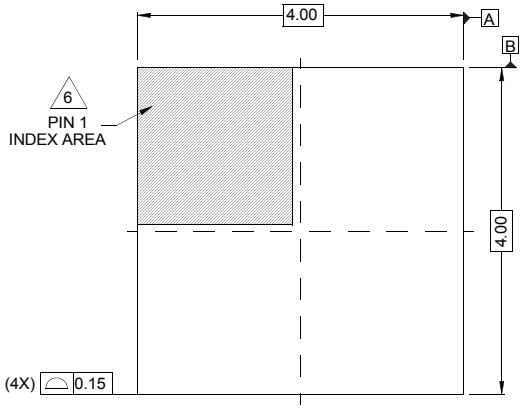
Si Gate CMOS

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

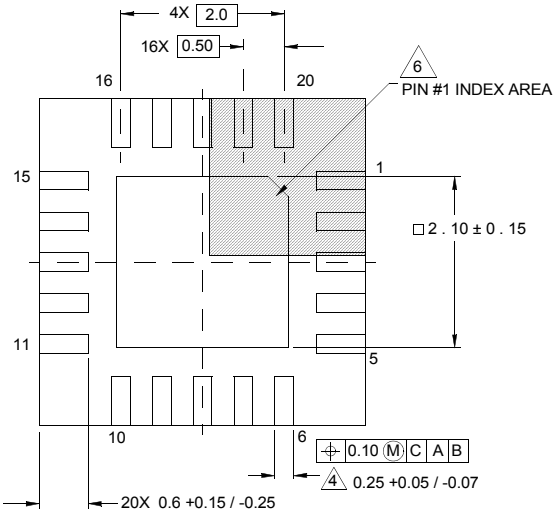
Package Outline Drawing

L20.4x4

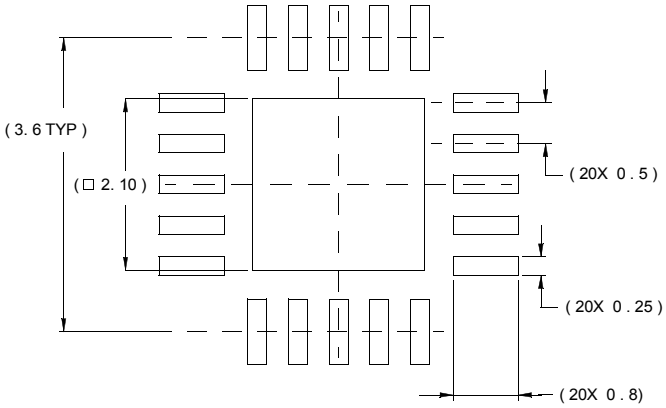
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 11/06



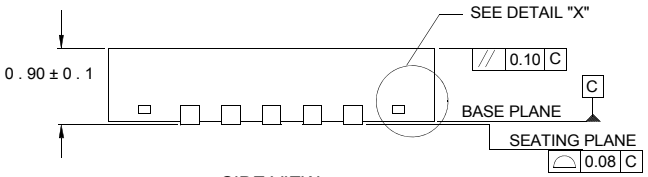
TOP VIEW



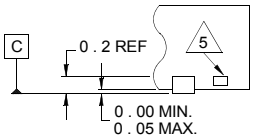
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.